The ZeroAMP project
– NEM Switch devices and packaging for harsh environments

Piers Tremlett, Microchip Technology Inc.

IMAPS UK webinar

Wednesday 12th Jan 2022

Introduction

- **Technical topics that will be covered**
  - MEMS processes for Nano Electro-Mechanical Switch (NEMS) technology
  - Wafer to wafer bonding
  - High temperature packaging

- **From System in a Package to System on a Chip**
  - Route to integrated MEMS sensors, logic and memory on a single chip?

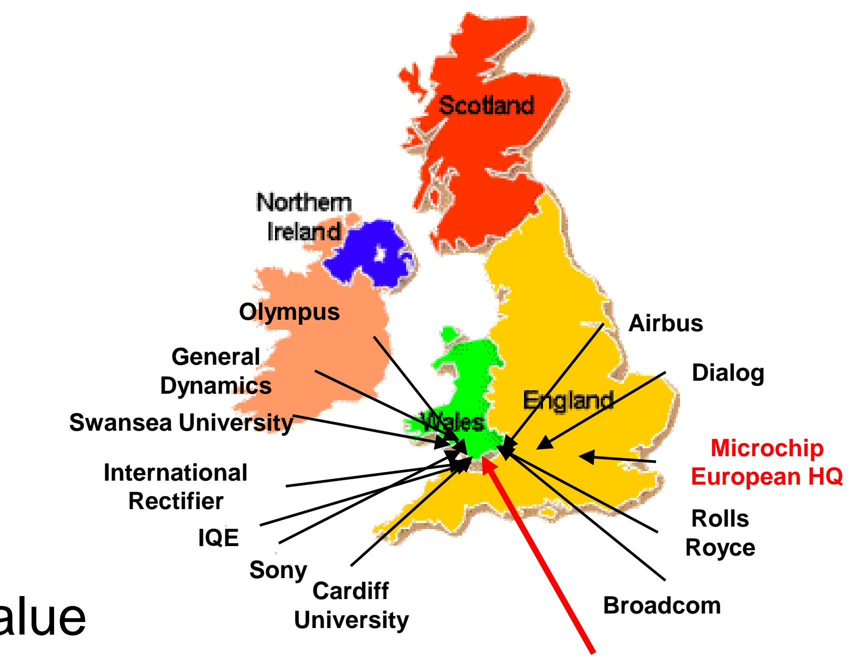
- **NEM switch applications**
  - Harsh environment data logging
    - case study of a solder reflow furnace profiling demonstrator .
  - Intelligent control system

The ZeroAMP project and Microchip

Microchip Caldicot site background

- Microelectronics factory
  - Established in South Wales since 1983
  - ~120 employees, 30,000 square foot facility

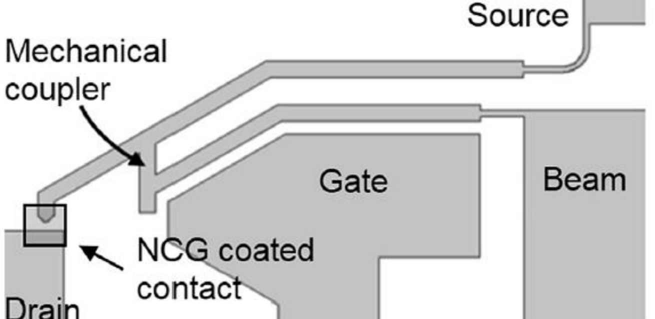
- Design & Assembly Expertise:
  - Surface Mount Technology, Chip on Board
  - Focused on solving complex problems that our customers value
  - High reliability customers

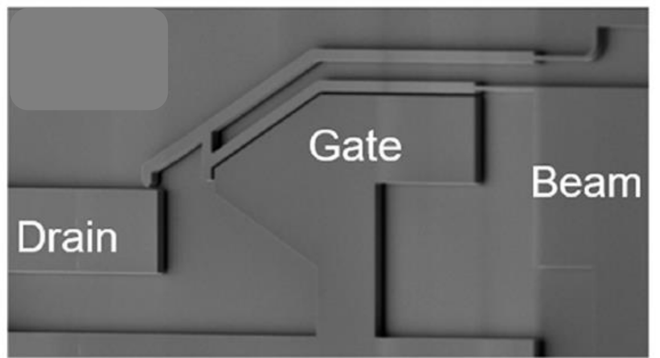


- *Specialising in “**Miniaturisation**”*
  - ***Expanding miniaturization into Harsh Environments***
    - ***High temperature***
    - ***High radiation***
    - ***Low energy availability environments***

Microchip Advanced Packaging

The ZeroAMP project





- ZeroAMP is a follow on project to NEMICA
- 7 partners
- 4 year H2020 project
- Started January 2020, finishes June 2024
- An Horizon 2020 funded by the EU
- To develop mechanical "transistors" using MEMS technology

NEM switch technology and devices

- Introducing basic NEM Switches
- Integrating NEM Switches to make logic and memory chips

Integrated MEMS digital transistors - NEMS

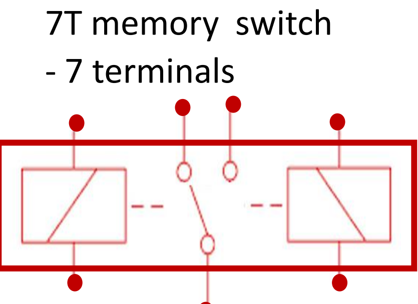
7T Non-Volatile Memory Cell

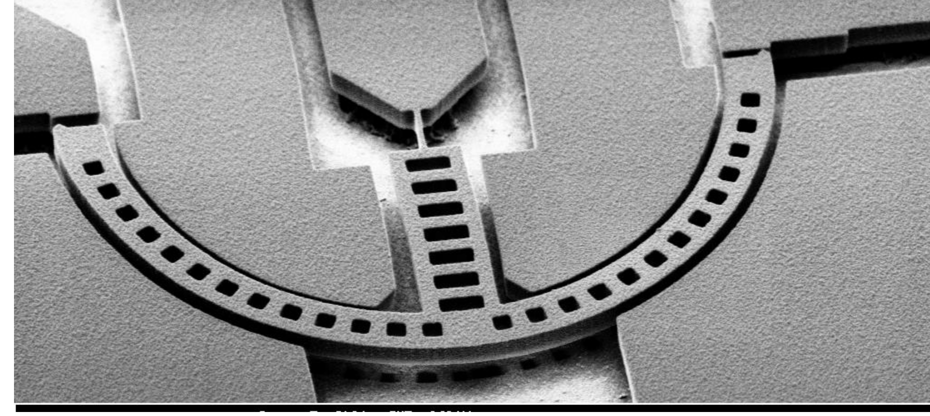
One Time Programmable (OTP)

&Programmable Memory eg sensor calibration data

- >340°C
- 100Mrad

7T memory switch
- 7 terminals





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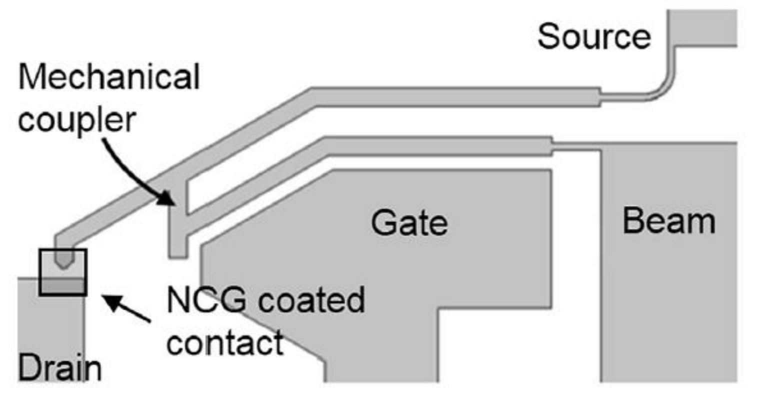
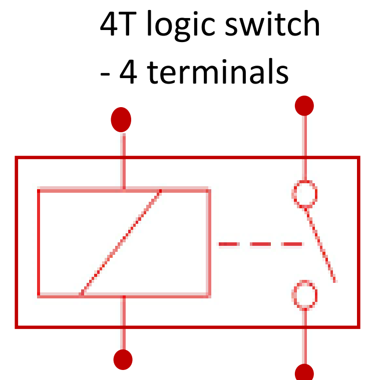
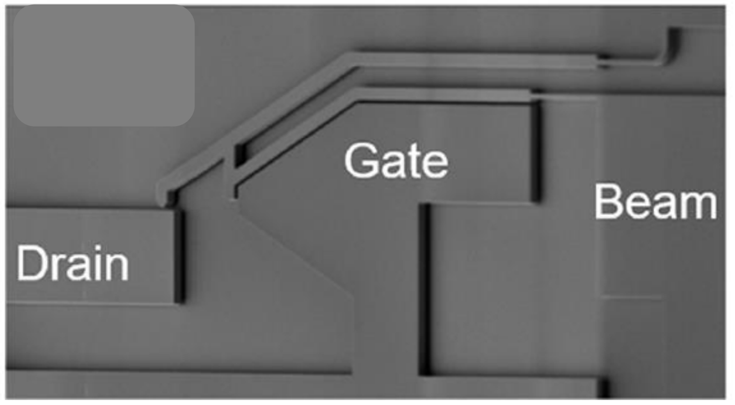
4T Digital Logic Gate

- very low current usage
- 50% low power CMOS



4T logic switch
- 4 terminals





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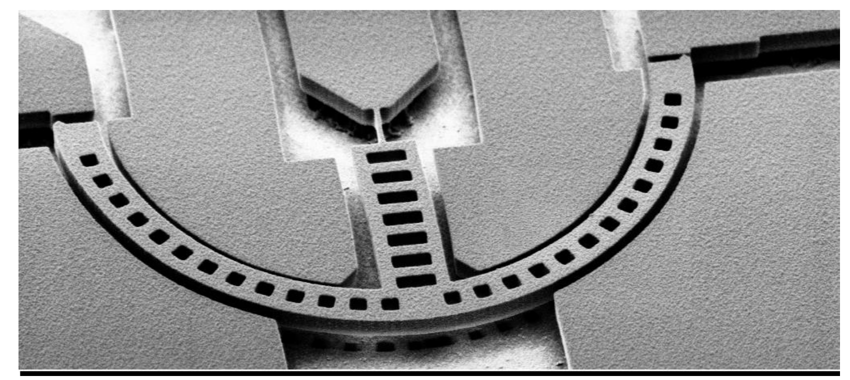
Outcomes and potential benefits of NEMS

- Memory cell
  - Memory state maintained by:
    - NCG contact tip - Van der Waals forces
    - metal tip - welding (de-weld and re-weld possible)
      - For One Time Programming OTP
      - and Multi-time Programming MTP



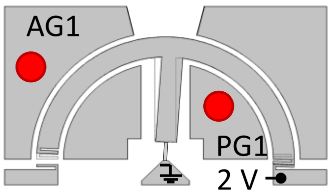
- Potential benefits
  - Rad hard and high temp calibration memory
  - Logic and Memory on one chip operating at up to 340°C (non von Newman architecture?)
  - Super low power < 50% of CMOS (and at temperature)
  - Low gate count FPGA’s

Initial multi-time programmable memory test

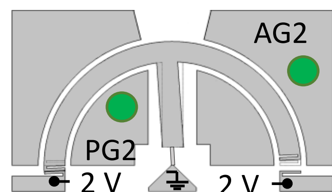
S. Rana, J. Mouro, S. J. Bleiker, J. D. Reynolds, H. M. Chong, F. Niklaus, and D. Pamunuwa, "Nanoelectromechanical relay without pull-in instability for high-temperature non-volatile memory," Nature communications, vol. 11, no. 1, pp. 1-10, 2020.

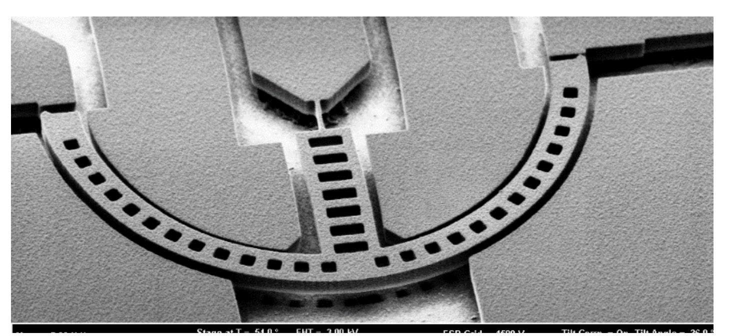
Cycling at 200 ^{o}C, in a vacuum ambient

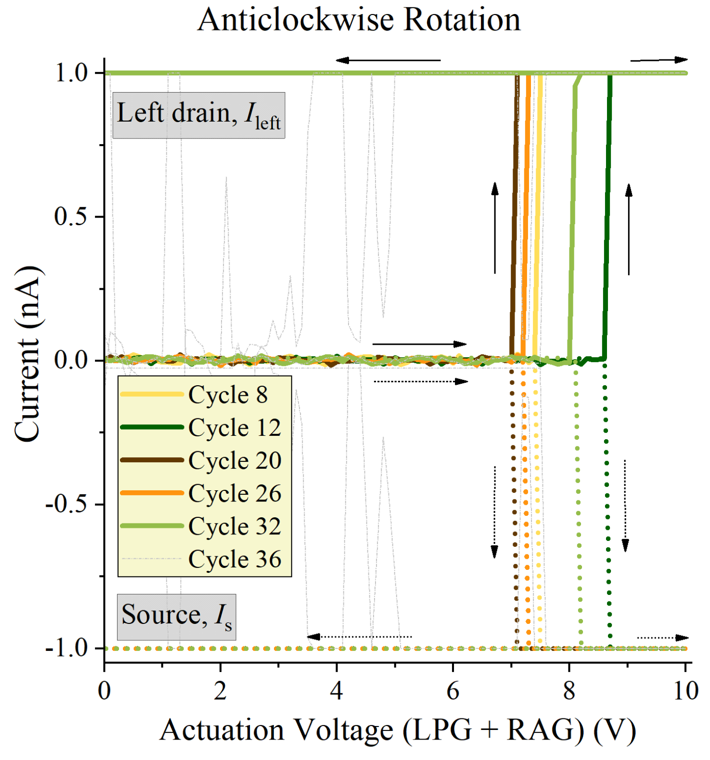
To rotate clockwise, apply voltage to principal gate 1 and auxiliary gate 1

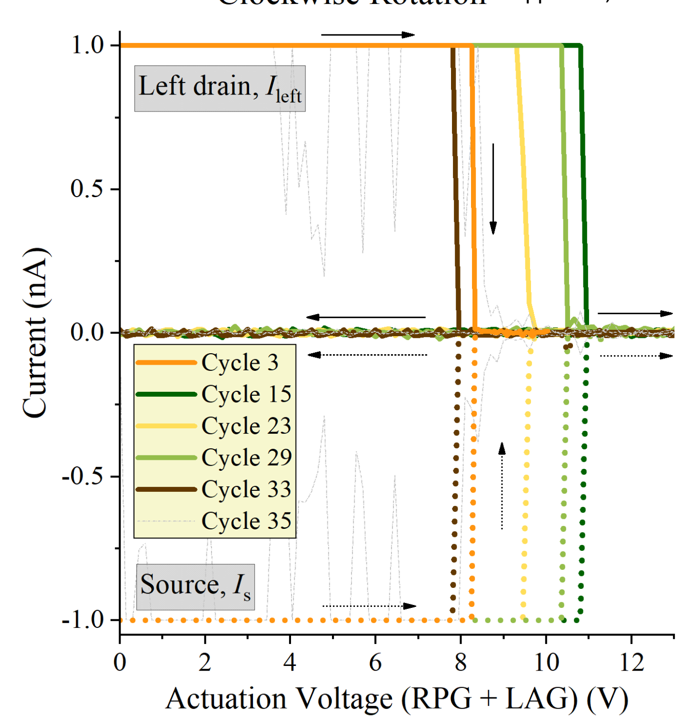


To rotate anticlockwise, apply voltage to principal gate 2 and auxiliary gate 2



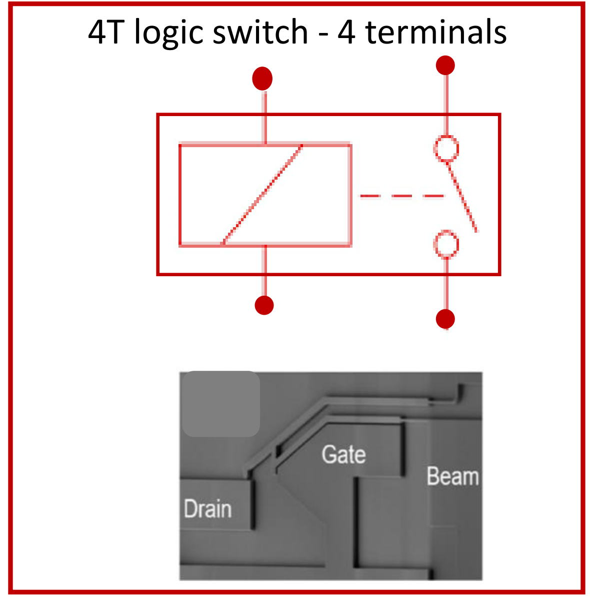


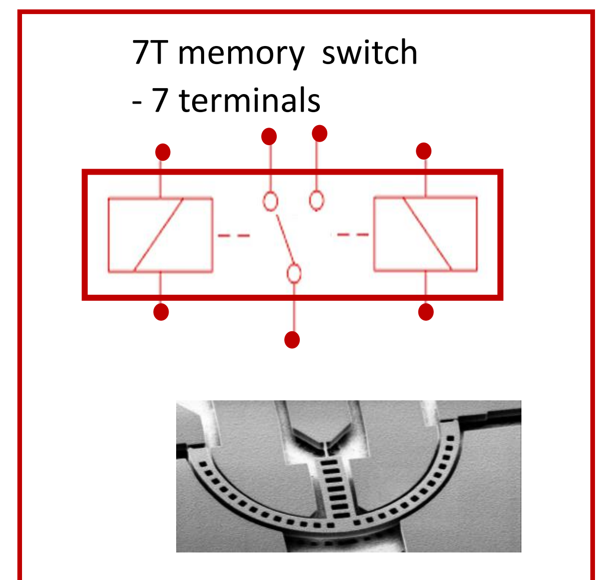




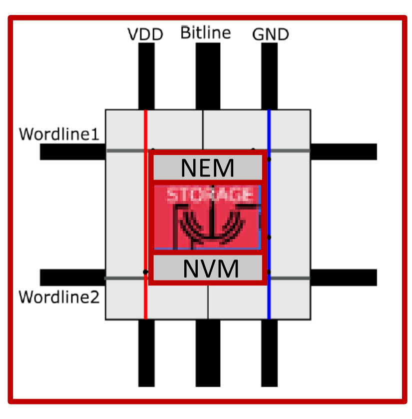
- **Once rotated, relay stays switched when voltages are removed (through stiction)**
- **State of relay (i.e. rotated left or rotated right) stores a '1' or '0'**

4T and 7T cells create logic and memory blocks

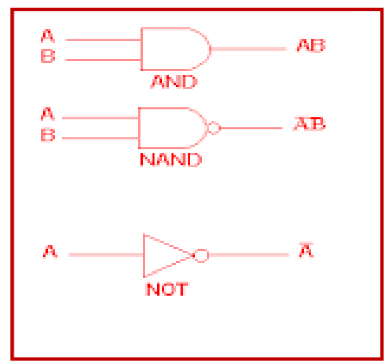




Addressable memory block and logic blocks made from 4T and 7T cells



1 bit memory block



Logic blocks

Memory die development

4T & 7T addressable 1 bit memory cell design

VDD
Bitline
GND
Wordline1
NEM
STORAGE
NVM
Wordline2

First real 1 bit memory cell
(95% of area taken by wire bond pads)

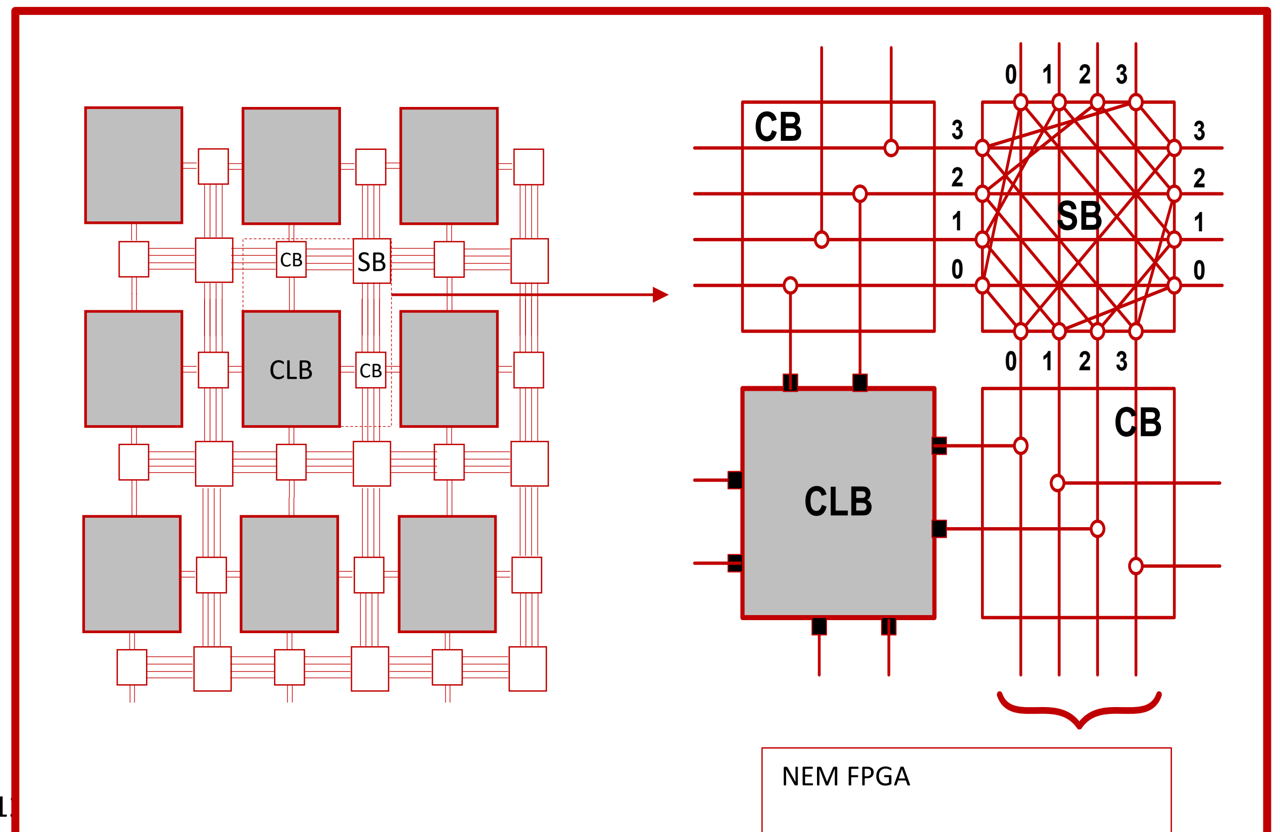
VDD
BL
GND
WL1
WL2
NVM Cell

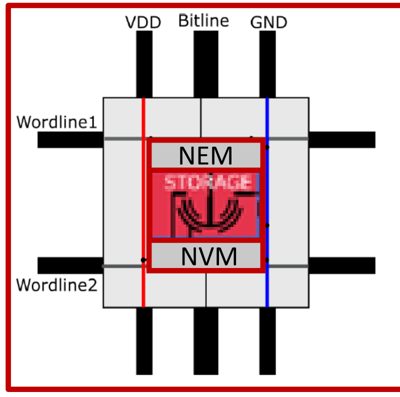
- 1 bit memory cell test chip
  - 4T addressing logic + one 7T memory cell
  - Tile-able configuration for larger memory implementation
- Simpler cell schematic than CMOS SRAM
  - Single voltage for read and write, fewer FETs/switches
  - Estimate that 256byte = 200 x 200um

Future FPGA plans for ZeroAMP

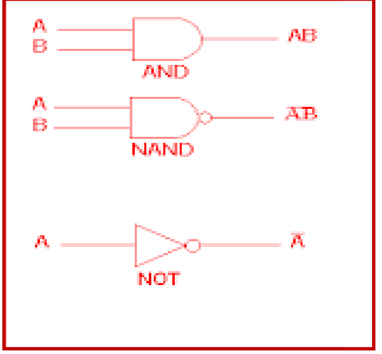
Zero AMP

- Develop a tile-able FPGA cell with:
  - Connector blocks
  - Switch clock
  - Configurable logic block





1 bit memory block

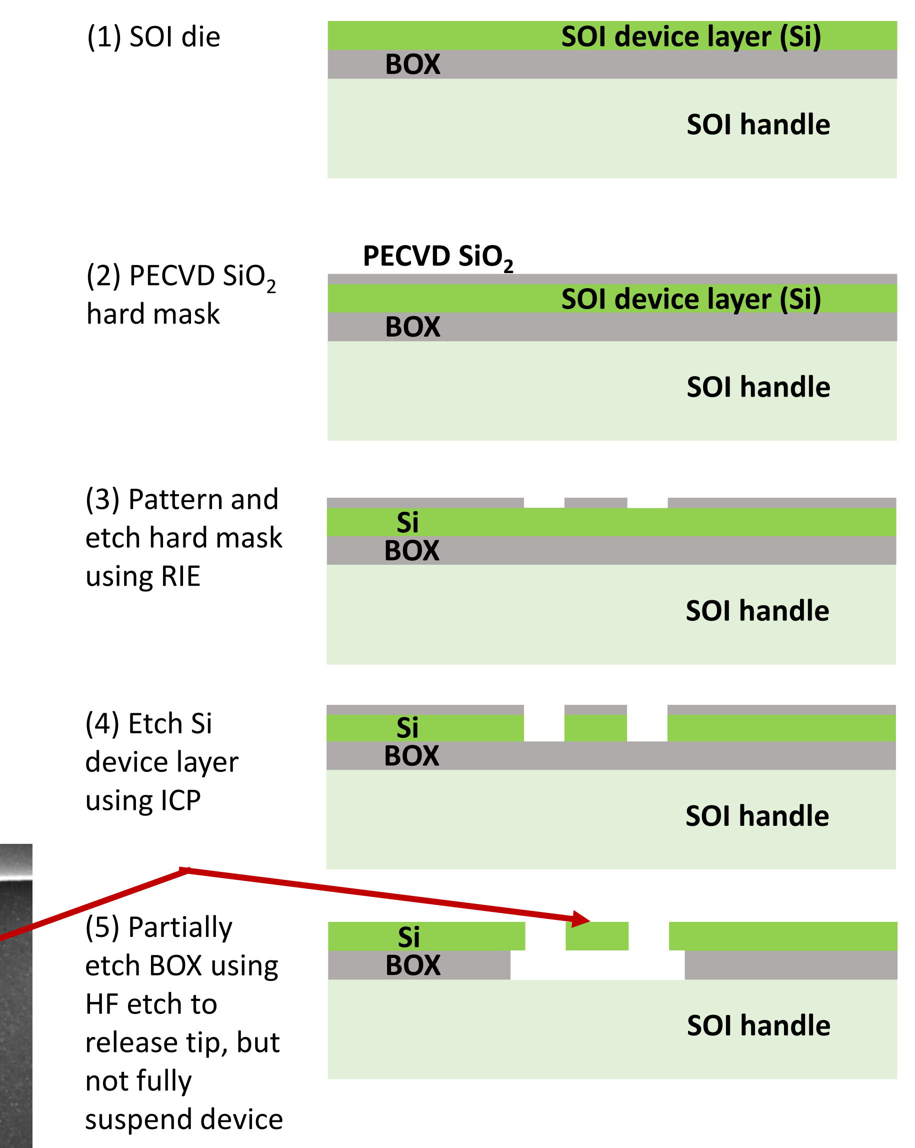


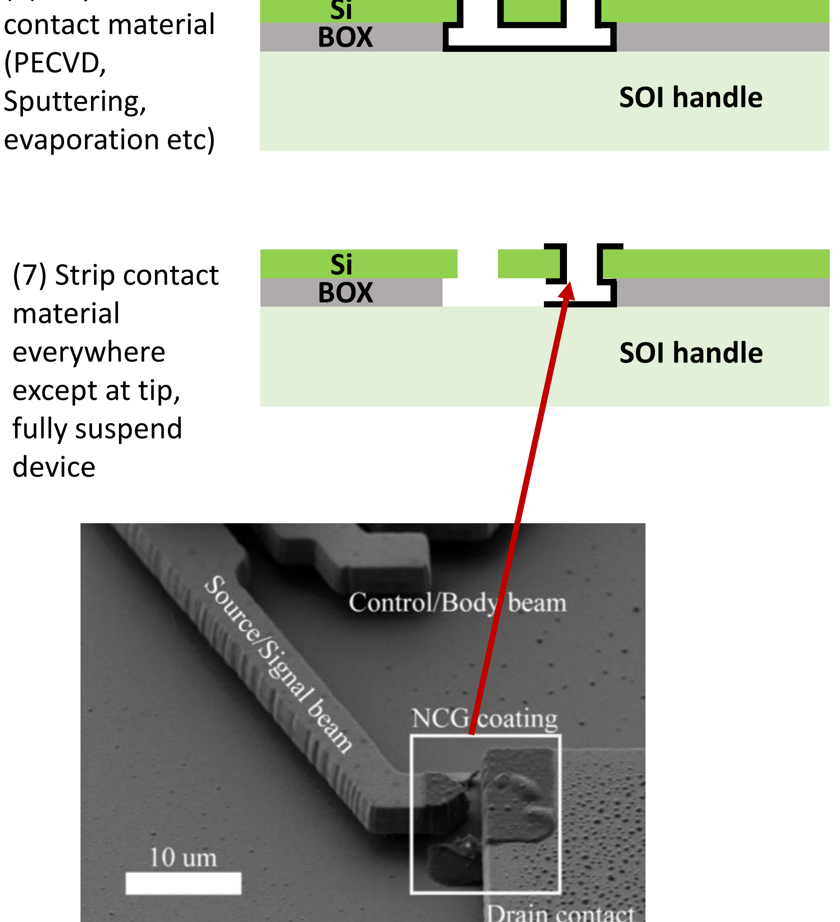
Logic blocks

NEM Switch foundry and backend processes

- NEM switch foundry processes
- Backend wafer scale process
- NEM Switch chip packaging

Basic NEM Switch manufacturing process

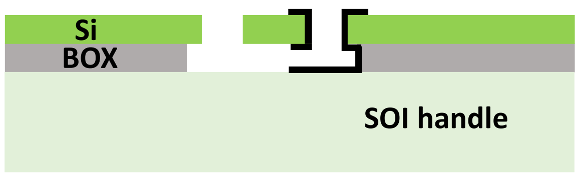


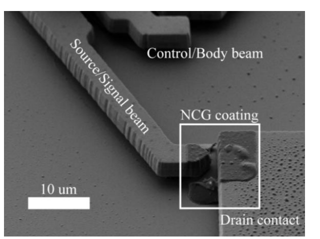


S. Rana, J. D. Reynolds, T. Y. Ling, M. S. Shamsudin, S. H. Pu, H. M. Chong, and D. Pamunuwa, “Nano-crystalline graphite for reliability improvement in MEM relay contacts,” Carbon, vol. 133, pp. 193-199, 2018.
https://www.sciencedirect.com/science/article/pii/S0008622318302549

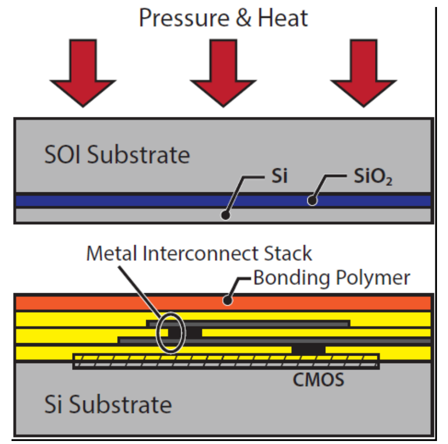
Wafer bonding to enable interconnections

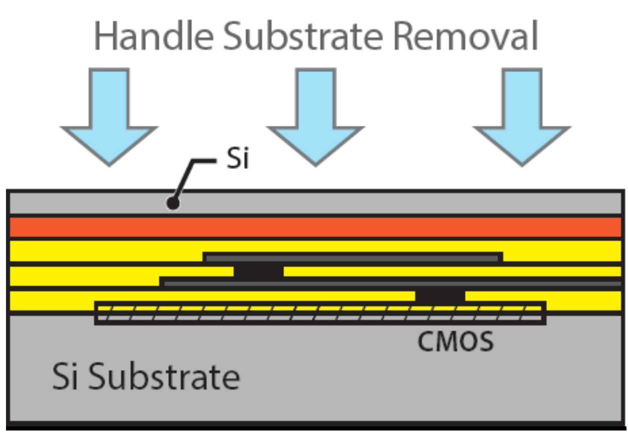
- Previous process only allows one interconnect layer





- Solution is to wafer bond an interconnect wafer
  - 1st wafer with full interconnect have now been manufactured





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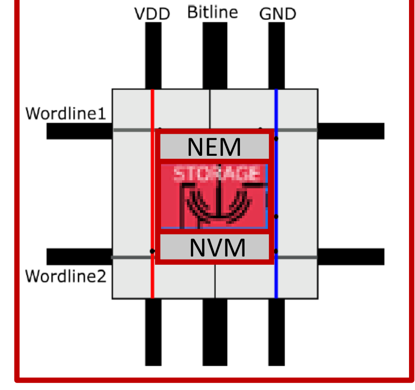
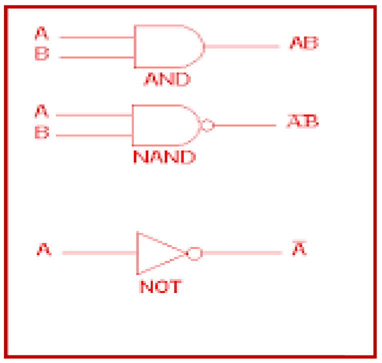
Summary of NEM Switch process activity

- Xfab have made the first interconnect wafers demonstrating the full interconnect process
- Logic and memory demonstrators to be fabricated onto these wafers shortly
  - Integrated Memory and FPGA chips to follow next year



1 bit memory block



Logic blocks

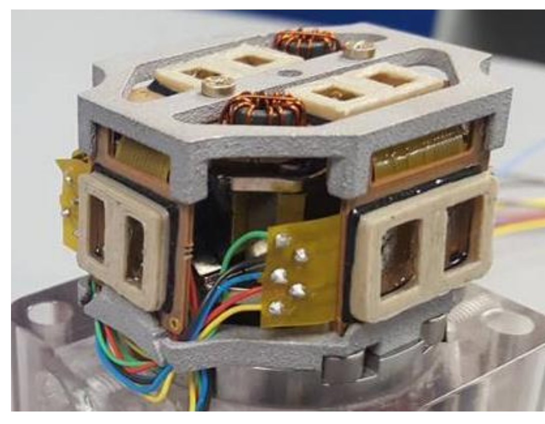
NEM Switch packaging and device integration

- Packaging is essential to the project
  - To realise the environmental capabilities eg functionality and reliability at 340C
  - Using System in a package o simulate wafer integration

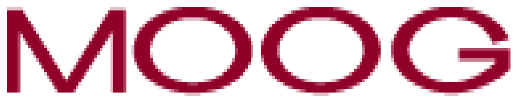
The NEMICA project

Innovate UK

- UK Innovate project to develop NEM technology
  - Leading to the ZeroAMP project
- Expected outcomes
  - 340°C MEMS based non-volatile memory
  - Control system for 175C jet engine fuel valve actuator

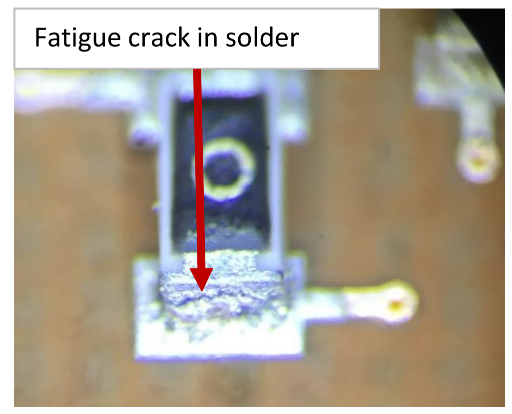


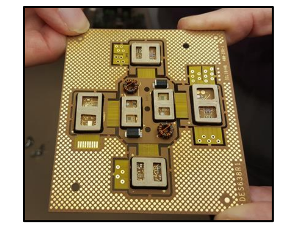
- Four partners

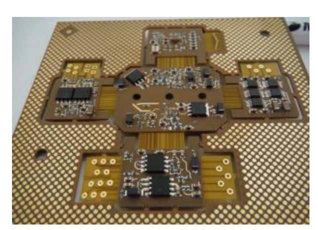


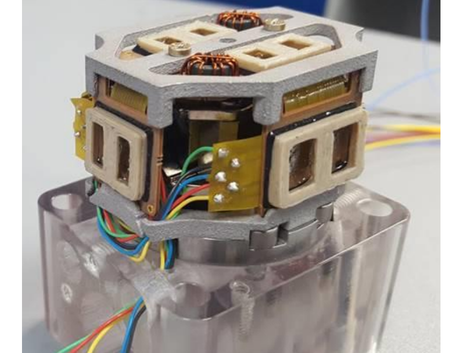
Organic substrate based CoB packaging from NEMICA

- A non hermetic CoB assembly system capable of sustained 190°C
- If hermetically encapsulated, capable of sustained 250°C
  - Beyond the melting point of solder
  - Alternative joining materials - better capability than solder
- Capable of extreme thermal cycling -55 to 175°C
- Used the advantages of flex rigid PCBs



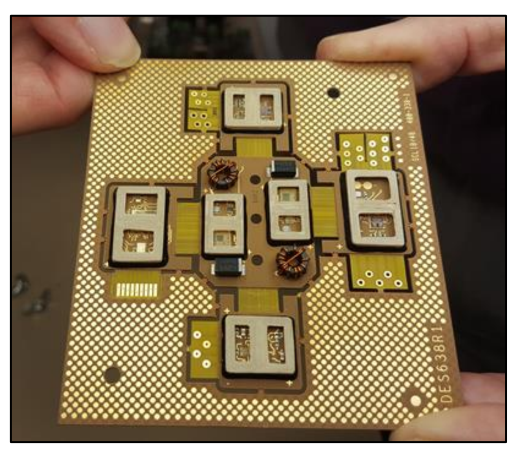


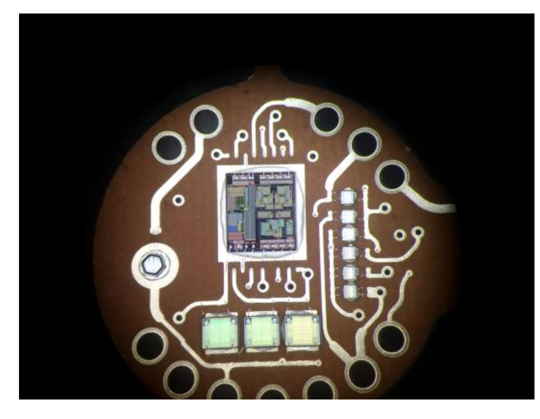


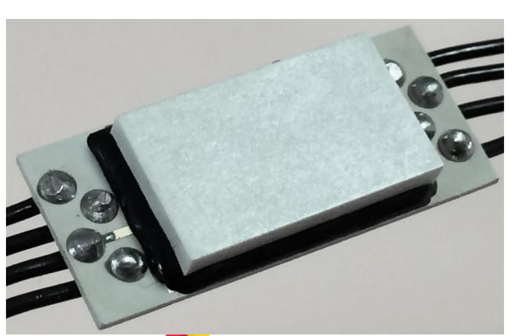


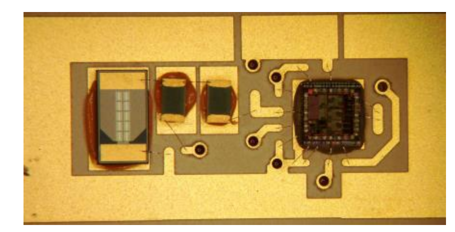
High temperature packaging

- Organic packaging from Nemica
  - Capable of up to 250C

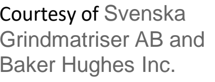


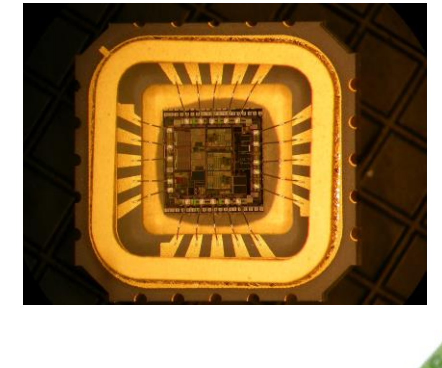






- Example ceramic packaging
  - Further packaging development
  - To aim to be capable of 340C



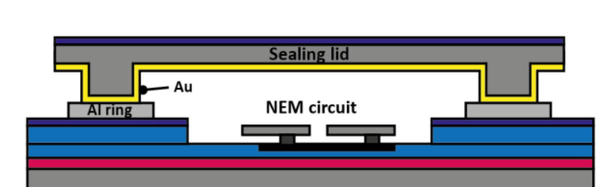


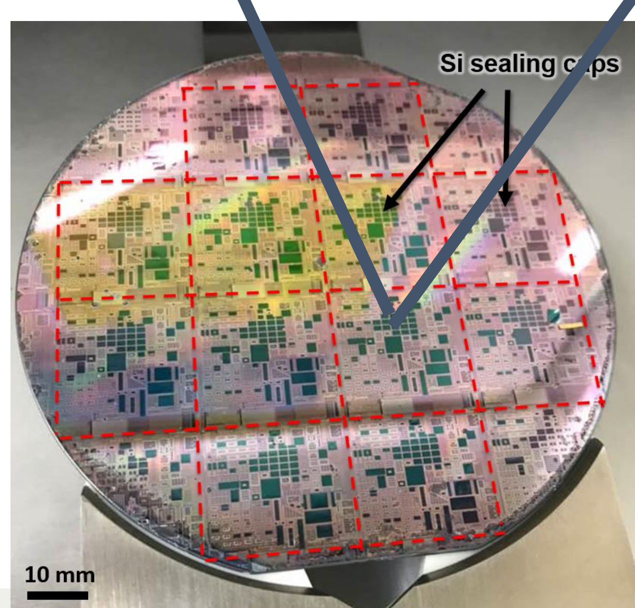
Courtesy of Svenska Grindmatriser AB and Baker Hughes Inc.

CONFIDENTIAL INFORMATION

Wafer scale packaging developed in ZeroAMP

- Wafer-level sealing by Au-Al bonding enables a hermetically sealed die cavity
  - Vacuum or inert gas filled



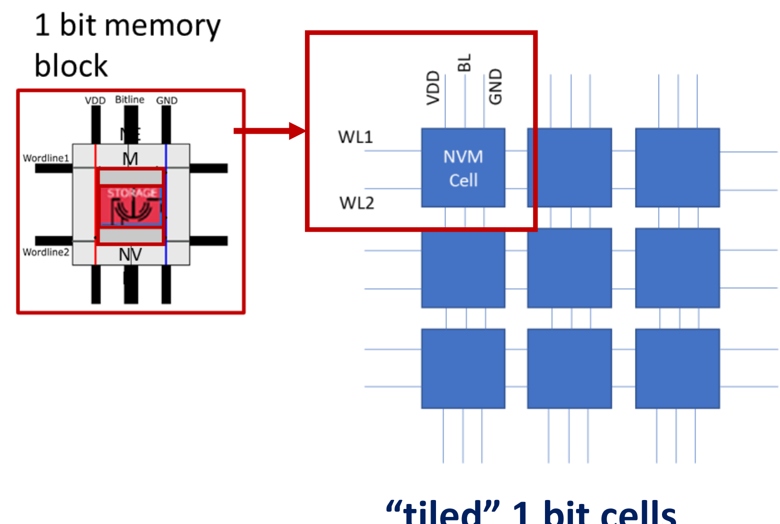


- Sealed cavity protects switches
  - Excludes O2 for a longer life
  - Easier to handle the die

- The project has successfully demonstrated wafer-level vacuum sealing.

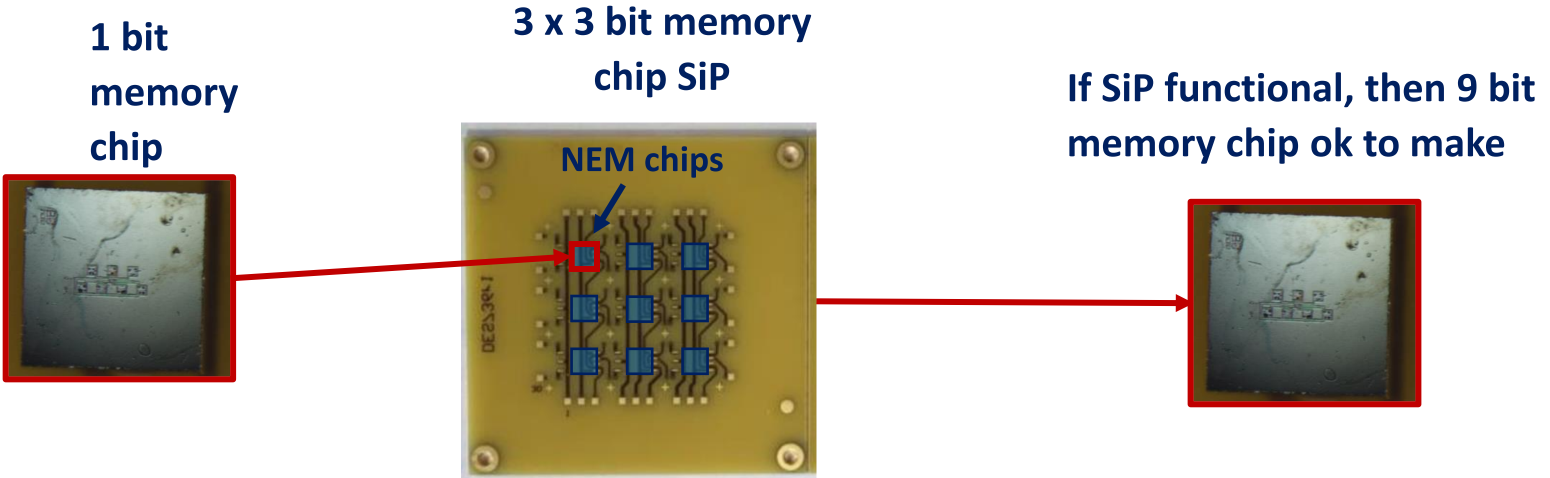
Accelerating chip and product development with SiP

- The single 1 bit memory is designed to be “tileable”
  - each cell can be individually addressed
  - by word lines 1,2 and the bit lines: WL1,2 and BL



“tiled” 1 bit cells and interconnects

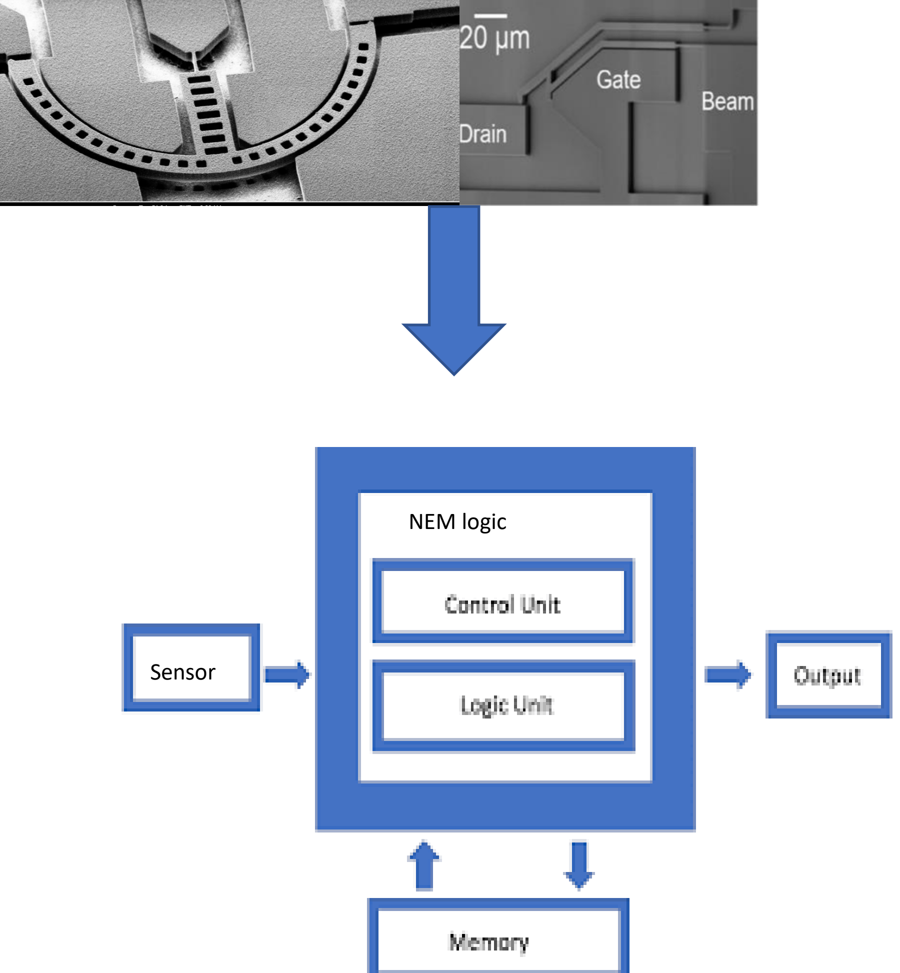
- Proving the tiling configuration of the memory cell with SiP
  - Do WL1,2 and BL address each memory bit successfully?
  - If “yes”, then ok to manufacture a 9 bit (or greater, 256Kbit?) chip



From single NEM switch cells to SoC (using SiP)?

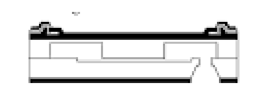
- Can we go from these NEM switches

- To a single chip containing
  - MEM sensors
  - Logic
  - Memory
  - For a fully integrated single chip MEMS system?



Sol sensor examples

- The following sensors might be integrated with NEMS logic
  - Flow and gas sensors
  - Pressure sensors
  - Resonators
  - Accelerometers



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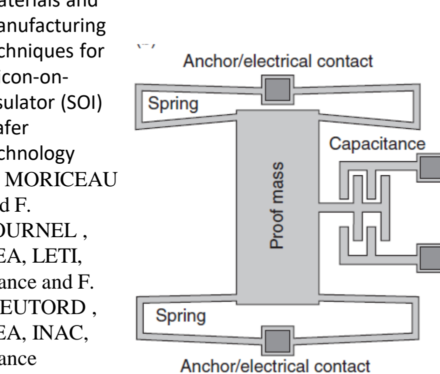
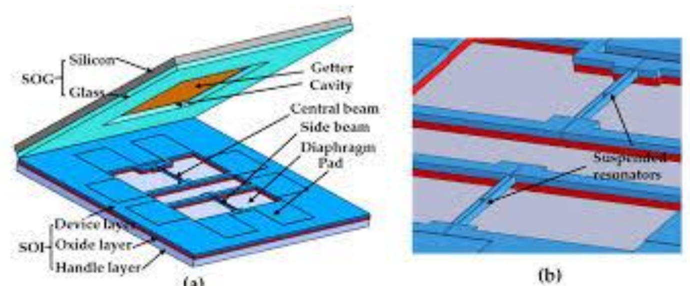
Materials and manufacturing techniques for silicon-on-insulator (SOI) wafer technology H. MORICEAU and F. FOURNEL , CEA, LETI, France and F. RIEUTORD , CEA, INAC, France





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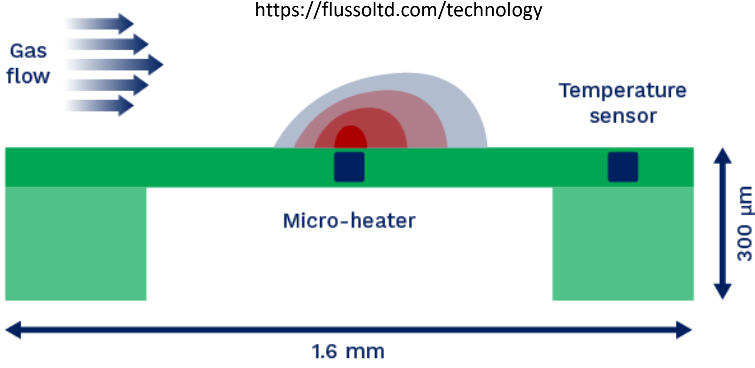
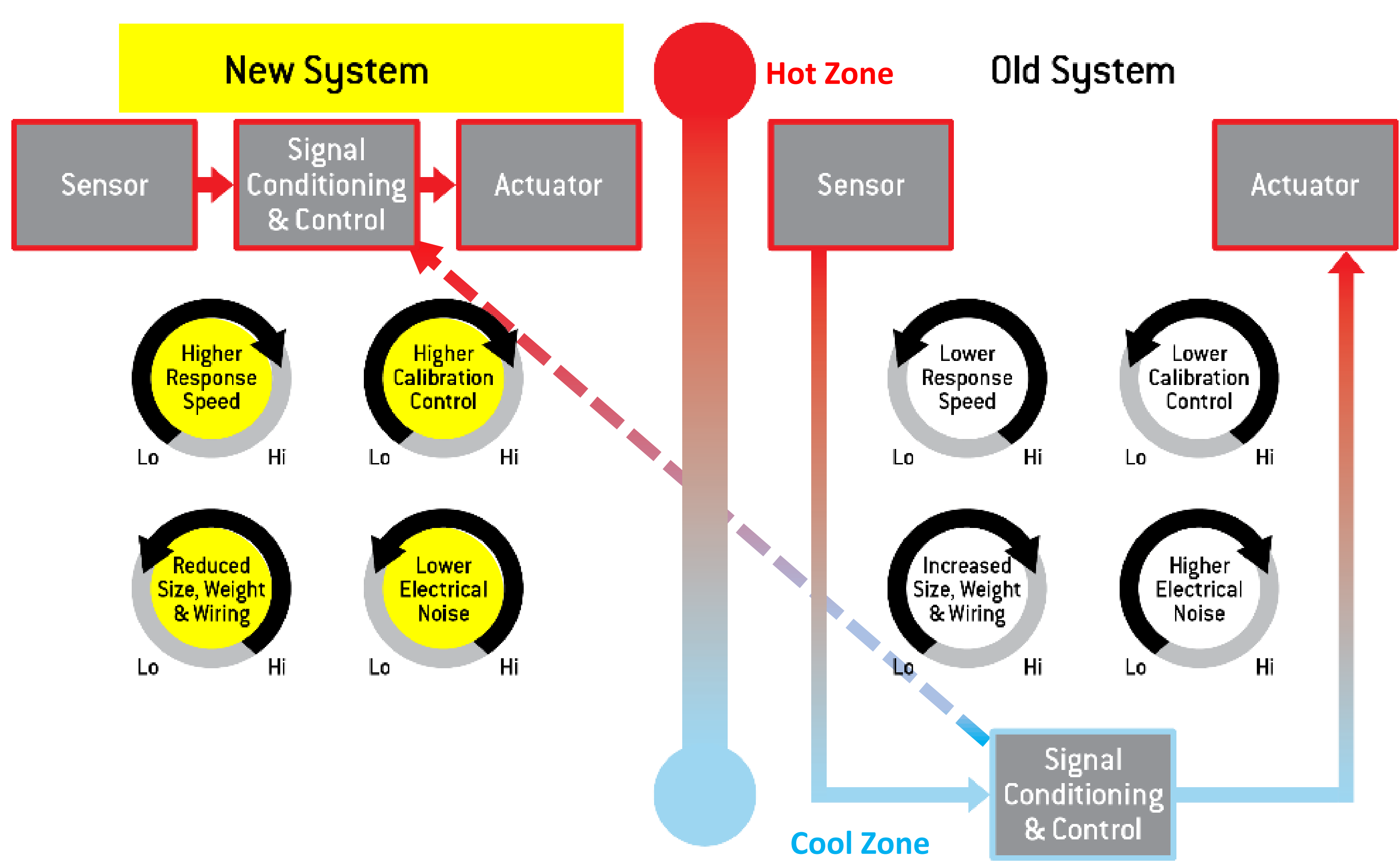


Applying ZeroAMP NEM Switch technology to applications

- Analysis of NEM Switch capabilities that point to application areas
- Example application – solder reflow profile monitoring

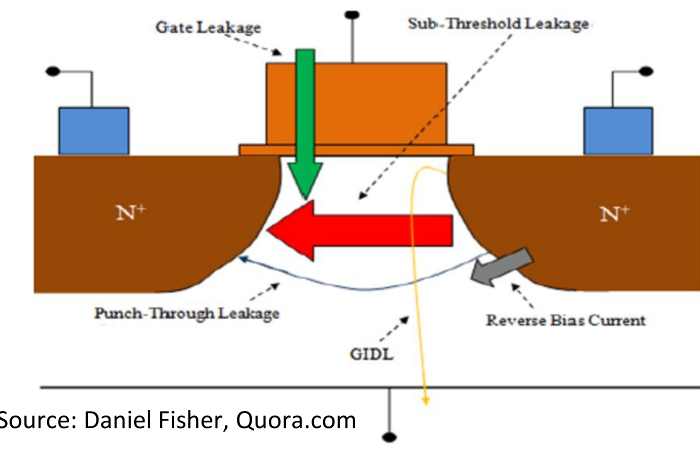
Original NEMICA application rationale

- Benefits of localising electronics for sensor / actuator control systems



Forever data collection…..anywhere

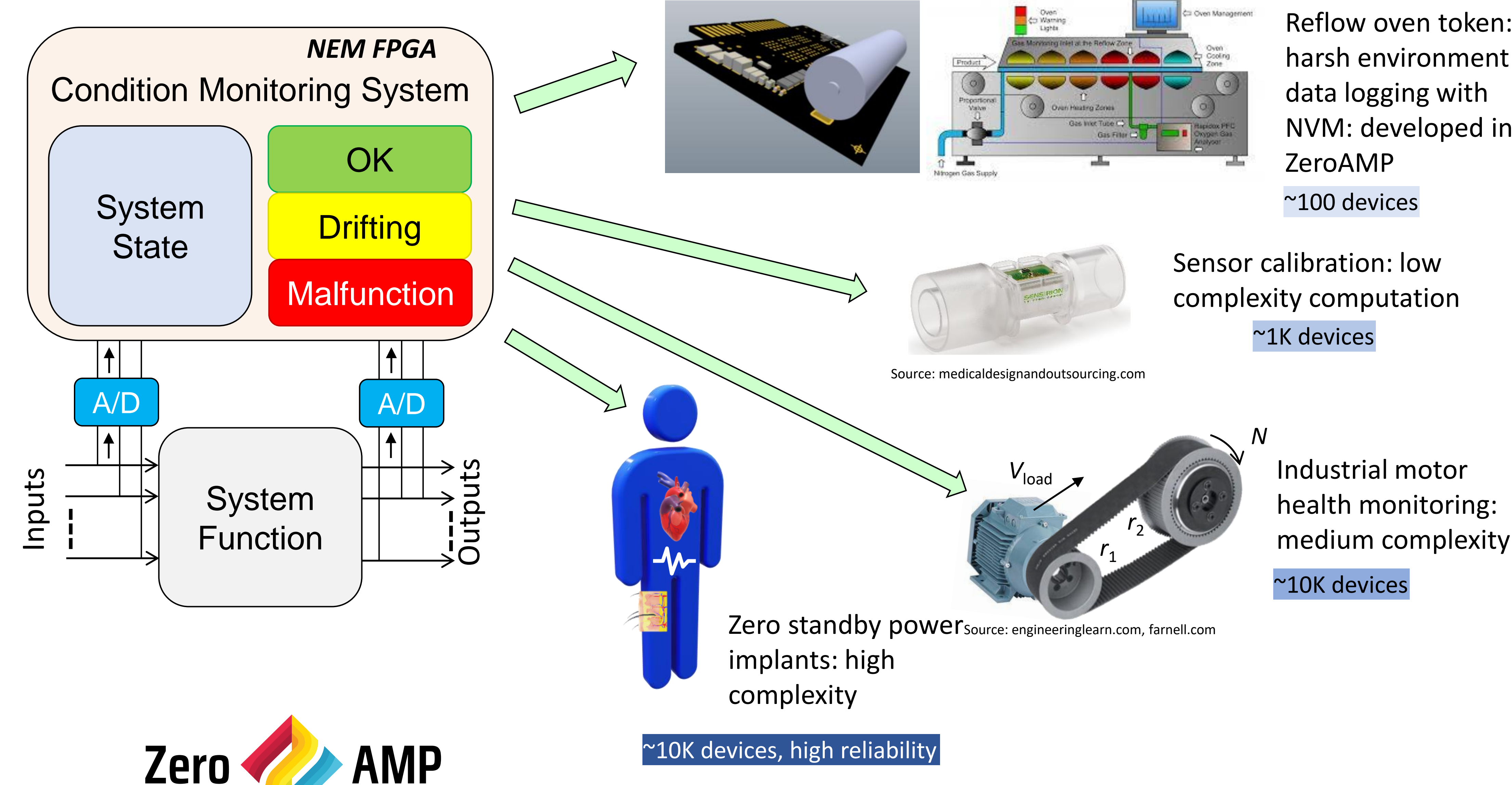
FET leakage paths



Source: Daniel Fisher, Quora.com

- CMOS devices
  - Leak and leak faster the hotter they get
  - Are susceptible to random radiation events
- NEMS devices
  - Retain their state forever – each switch held shut by Van der Waals forces….or welding
  - Unaffected by temperature or radiation to much higher levels than CMOS
  - Offer single chip integration of memory, logic and sensor
- **Data can be collected and kept forever no matter the environment or lack of power**

An intelligent system control approach - Context Aware Monitoring

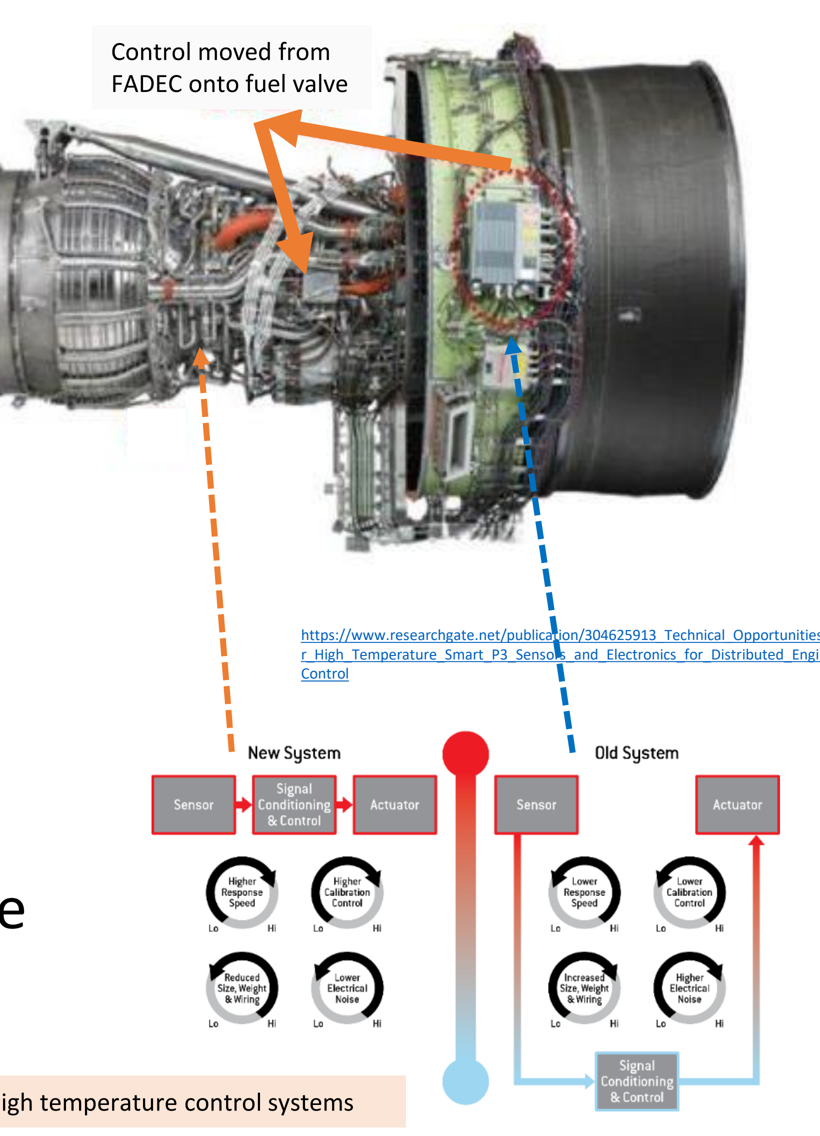


Nemica "on fuel valve" control – a context aware system

- Jet engine manufacturers now rent thrust/ hour
    - Uptime and efficiency are paramount

- Benefits of moving the valve control
    - Local control allows more wires for more sensors
    - More bandwidth for control improves efficiency
    - Health monitoring possible - to help uptime
    - Realisation of DEC (distributed engine control)

- NVM for boot up memory?
    - 175C environment is just OK for CMOS NVM (Non-Volatile Memory)



Understanding NEM strengths

- Using overlapping strengths to find applications

Product or applications environment

High radiation level environments

Extreme temperature environments

Low power availability environments

Extreme ambient temperature, hot or cold

Extreme temperature fluctuations

Triple overlap,

Best applications here?

Satellites?

Double overlap

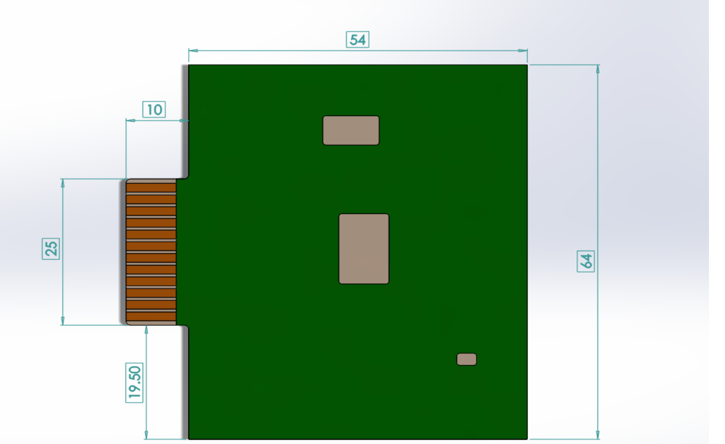
Good products here

Industrial?

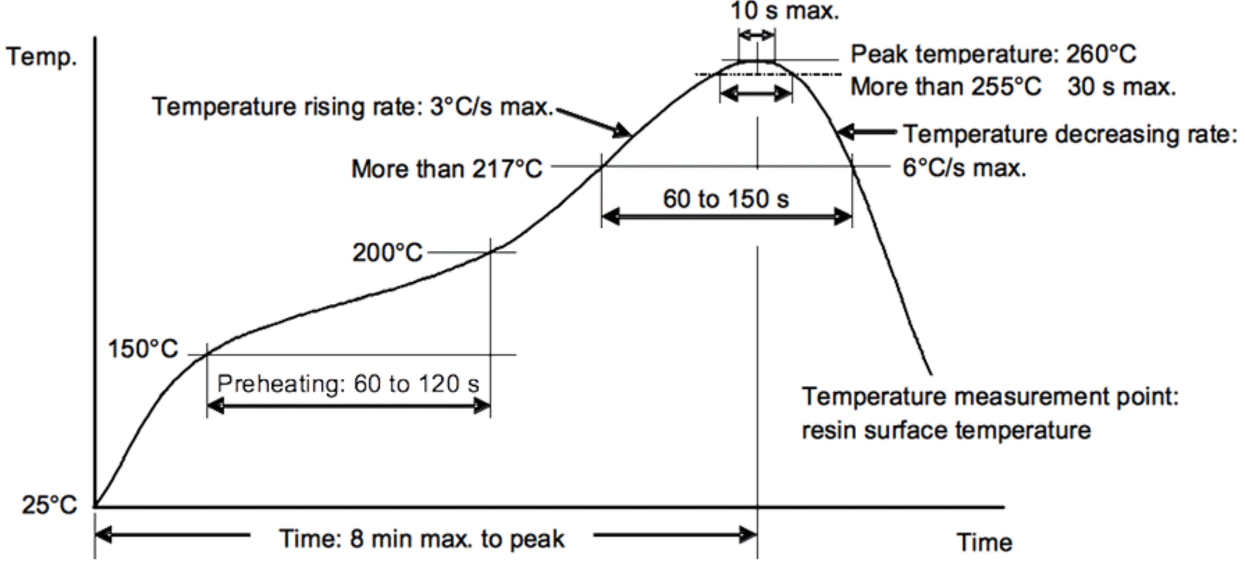
1) Difficult to access areas – expensive to access
2) Few or poor power sources - batteries for 150C to 340C
3) Weight or space of power sources is challenging and expensive

Example application - industrial temperature recording “Token”

- Example application – solder reflow profile monitoring



NEMS high temperature Token



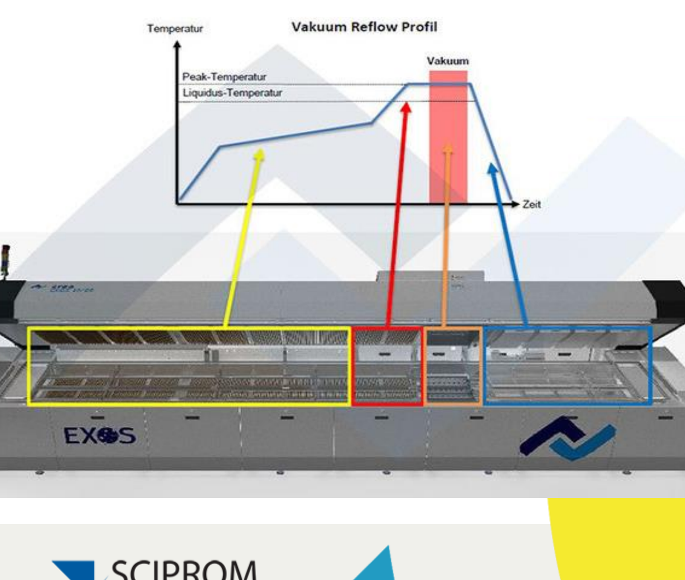
Tantalum capacitor power supply

Edge connector to download data

NEMS memory and FPGA

Temp sensor

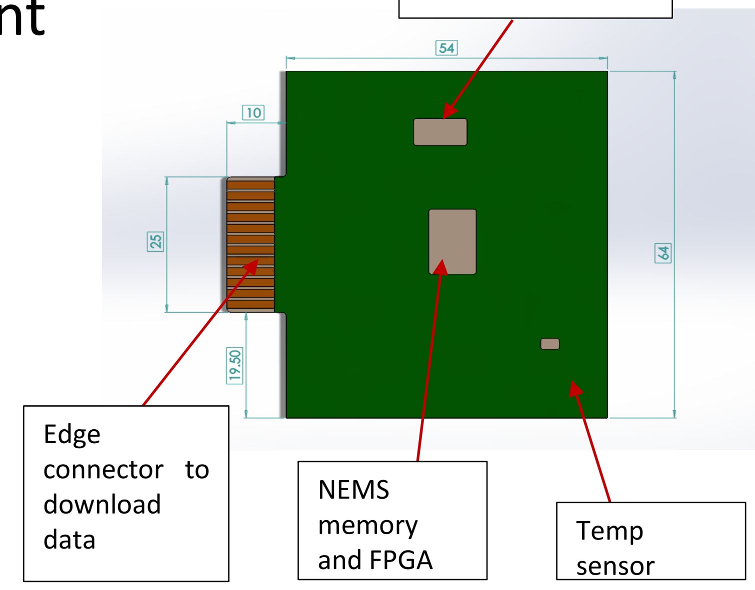
- Monitoring process temperatures - industrial belt ovens
  - Temperature monitoring token travels with normal product
  - The token records the dynamic temperature profile

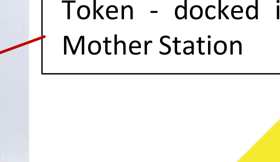


NEMS for harsh environment sensing

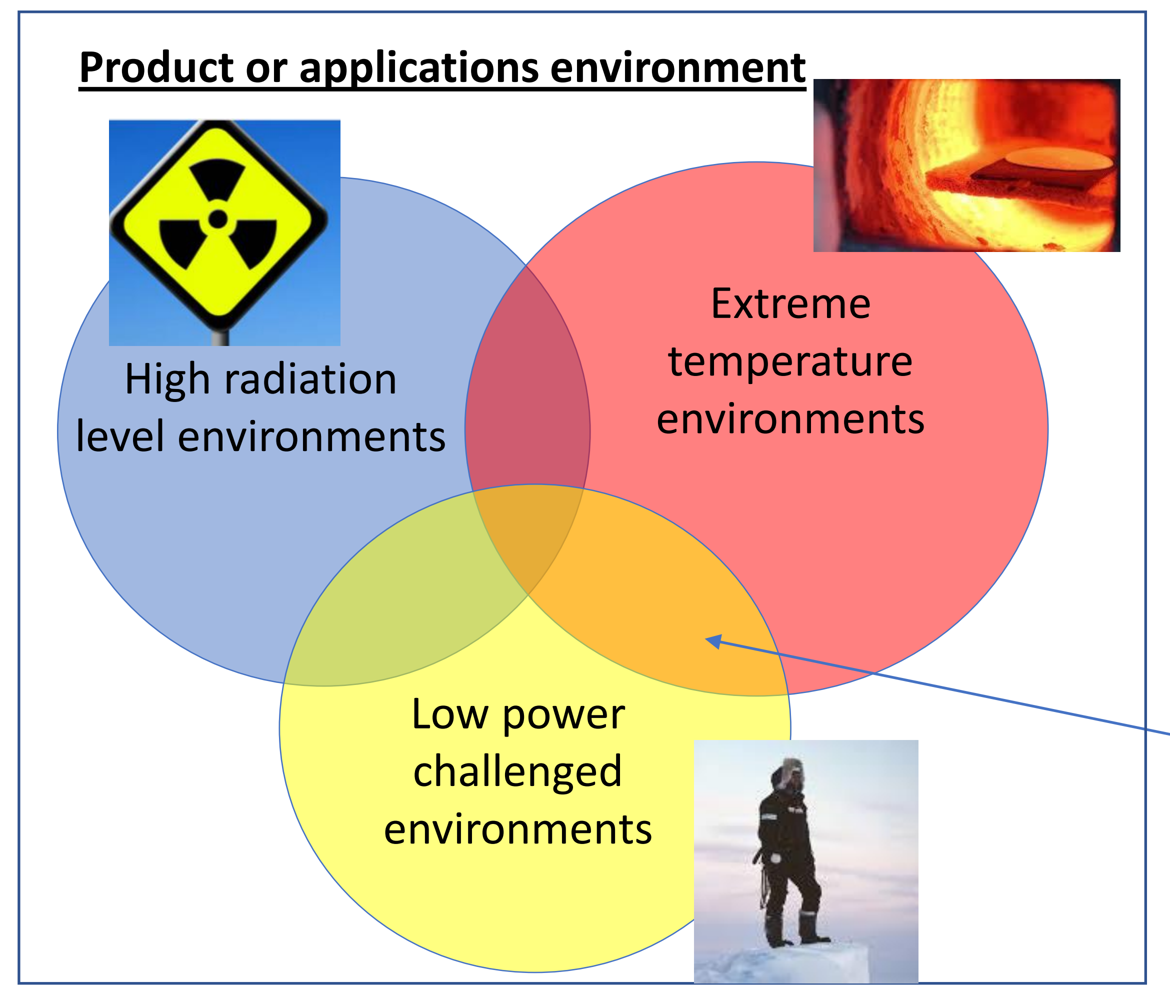
- Problems with wireless sensing in high temperature environment
  - Charge leakage in semiconductors
  - Lack of batteries for 150C to 340C temperature range
  - High temperature is usually within a metal box – RF shielding

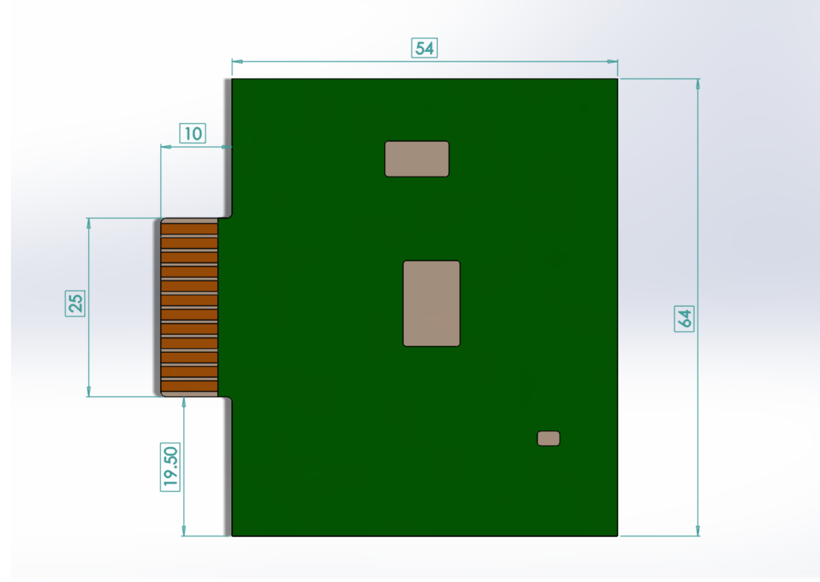
- NEMS solution
  - Use Caps / super caps + NEM switches chips?
  - Download data from Token to mother station
  - Reflowing product does not have to stop – SPC possible
  - Token emerges cold, normal metal box needs gloves





Temperature recording "Token"





Token uses the overlap of these two characteristics of NEMS devices

- 25C to 250C
- No battery power supply

ZeroAMP project presentation summary

Summary

- ZeroAMP NEMS technology is aiming to deliver:
  - rugged memory, logic and FPGA computing
  - capable of working at up to 340C and 100MRad

- On the way it is developing novel packaging
  - high temperature packaging
    - organic packaging capable of 250C
    - ceramic packaging capable of 340C
  - System in a Package to simulate and speed up chip design and development

- It aim to deliver products for data collection and system control that are rugged, long lasting, intelligent
  - The future vision is to integrate NEM switch technology and MEMS devices

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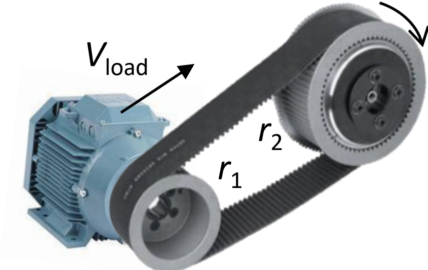
www.Zero-AMP.eu

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 871740 (ZeroAMP).

END

Context - Computing at the Edge of the Network

- Many industrial / IoT applications have a mix of harsh environment and very low energy requirements with need for simple processing. Eg:
  - Data logging in harsh environments
    - High-temperature manufacturing environments (furnaces, reflow ovens, production lines)
    - Downhole applications
  - Digital sensor calibration
    - Sensors used close to engines, motors, hot sites
  - Condition monitoring in high temp. / radiation environments
    - Log readings and generate event-based responses
- Transistor based solutions struggle because of some combination of environmental and energy limitations



Source: engineeringlearn.com, farnell.com

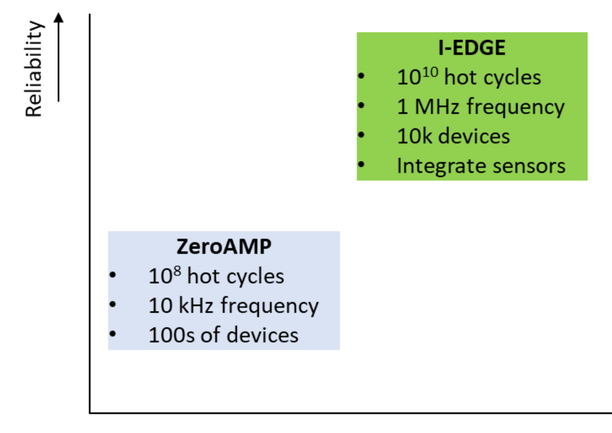
Hardware Platform for Edge Computing

❑ Produce a NEM FPGA demonstrator

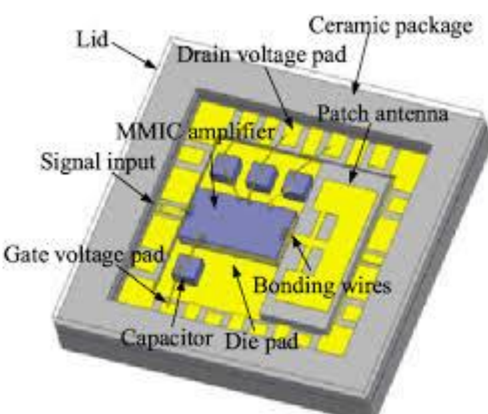
- Reprogrammable FPGA with embedded NVM, retains programmed state on power off
- Best in class harsh-environment capability: 300 ºC operation, 5 Mrad absorbed dose, zero standby current
- Very efficient implementations for conditioning monitoring
  - Reduced device count, vastly reduced latency for memory access
  - More programmable interconnection links for more efficient mapping of controllers, dynamic partial reconfigurations

❑ Advance NEM relay-based technology platform to TRL 4-5

- Flexible BEOL integration platform for die-level integration of NEM switches (logic and non-volatile memory) with any of the following combinations:
  - X-FAB CMOS interconnect stack (for dense integration of NEM switches): logic and memory chips for harsh-environment, zero standby power operation
  - X-FAB CMOS interconnect stack + devices: hybrid NEM-CMOS chips for zero standby power, selected harsh-environment constraints
  - MEMS sensors: Fabrication flow compatible with integrating wide variety of MEMS sensors, either on same die as NEM logic, or through 3-D stacking



Si
BOX
SOI handle


Lid
Ceramic package
Drain voltage pad
Patch antenna
MMIC amplifier
Signal input
Gate voltage pad
Bonding wires
Capacitor
Die pad

Single cell die

WL1

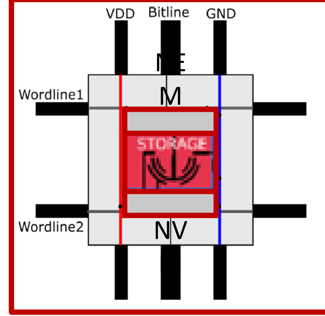
WL2

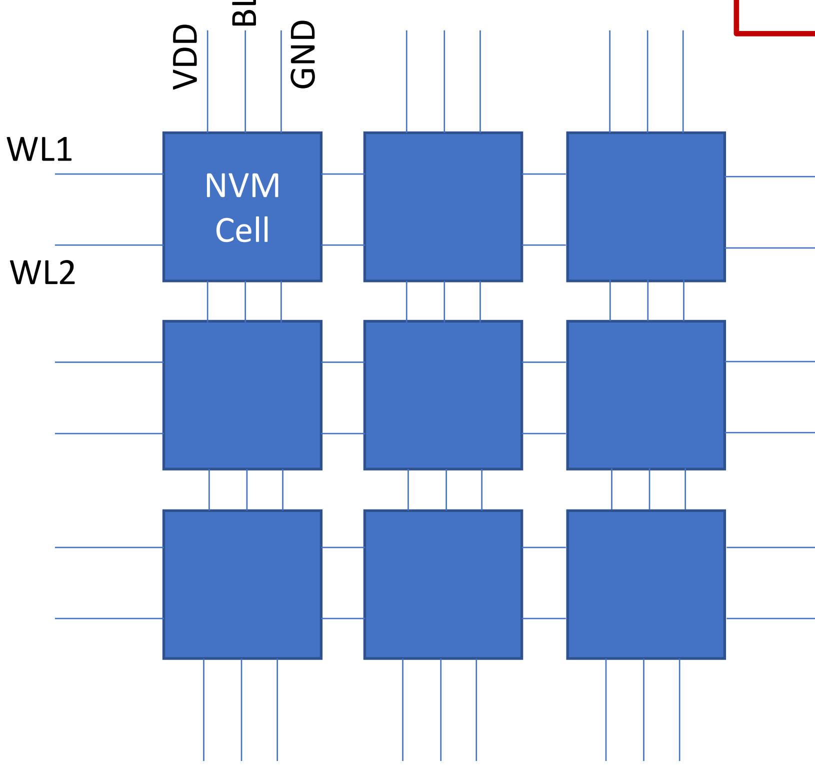
VDD

BL

GND

NVM Cell





MICROCHIP xfab AMO

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