ZeroAMP – Logic, Memory, Sensors and More for Harsh Environments

The ZeroAMP Integration Approach

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Zero AMP ULTRA LOW-POWER COMPUTING WITH SURVIVAL SKILLS

Outline

- How does the ZeroAMP integration approach affect sensor integration and system design?
- What are the main options?
- ZeroAMP's integration concept today…
- … and how it will evolve in the future
- How will this transition take place…
- … and what does it mean for sensor applications?

Sensor Integration/ System Design & Integration Approach

- Unique zero leakage power, high temperature, high radiation platform for ICs
- Hence, ZeroAMP´s technology can address a wide of sensing challenges where the use of conventional CMOS-based electronics is difficult or even impossible
- For convenient sensor integration and system design this platform needs to be
  - Flexible, adaptable to a sensor´s output signal levels, etc.
  - Easy to integrate in existing, PDK-based circuit and system design environments
    - Circuit and system designers can use a cell library to create the functionality they need and do not have to deal with individual NEM switches and their design or fabrication
- The ZeroAMP integration approach must allow for an easy interaction of its NEMS circuits with sensors and vice versa.

Sensor Integration using a common Interface

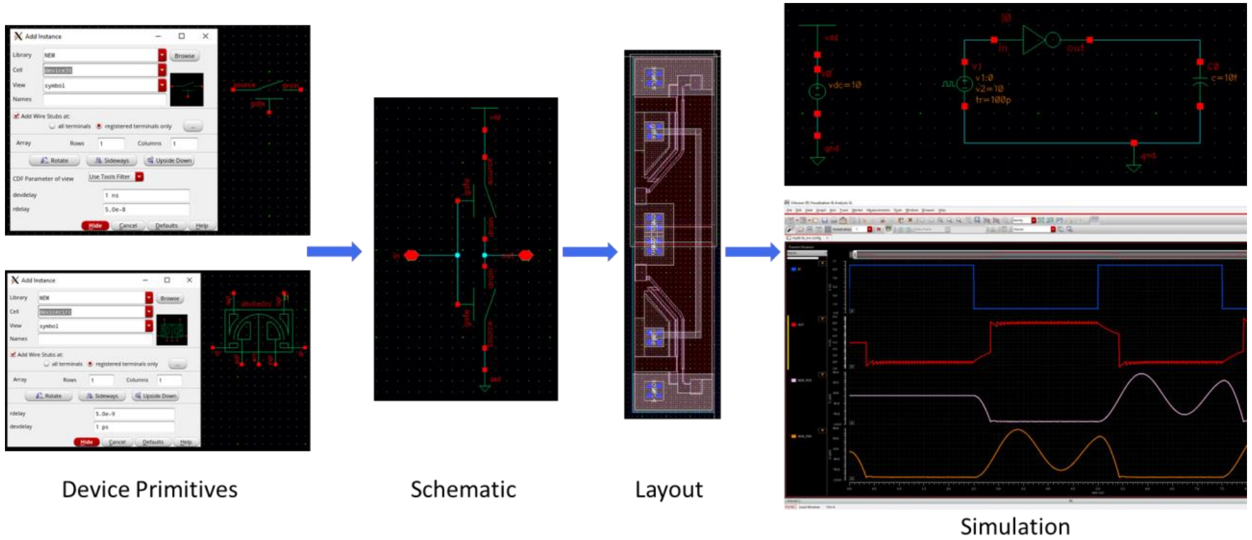
- System containing sensing elements and ZeroAMP's NEMS circuits build by using discrete sensors and discrete NEMS circuits
- Each developed and fabricated independently
- Each fully packaged
- Combined using a common interface to exchange control signals and sensor data
- Benefits
  - Highly flexible
  - Individual optimization always possible
  - Each element can tread the rest of the system as a set of black boxes
- *But:* Systems must be built as a set of individual components with electrical interfaces, no full Systems-on-Chip (SoC) possible

Monolithic integration

- For some sensing challenges and application scenarios the actual sensor can be monolithically integrated on the same chip as the NEMS circuits used for control, memory and read-out
  - E.g. a RTD temperature sensor
  - Fabrication flow for the NEMS circuits and the actual sensor need to be well-aligned
    - Starting with basics such as the SOI substrate…
    - …and not ending with the temperature budget of the overall fabrication process flow
  - Hence, optimization of each component of the system becomes more complex and interlinked
- *But:* Systems-on-Chip (SoC) and Systems-in-Package (SiP) become possible, the whole sensor system, including control, memory and read-out, can become just one single component

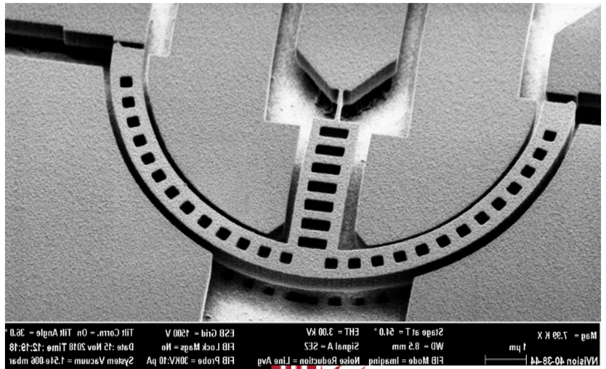
Where are we now…

- Circuit and system design
  - Using the software toolkit presented in morning session
  - PDK with a growing standard cell library



Where are we now…

- Fabrication
  - Utilizing a CMOS foundry wafer‘s interconnect stack as basis
  - Lab-scale processing by various partners at different locations
  - Use of rapid prototyping techniques such as electron beam lithography (EBL)
    - High degree of flexibility
    - Fast turnaround times
    - *But:* Low throughput and high costs per device
  - Reliable deposition and subsequent processing of a contact material guaranteeing long lifetimes for NEMS circuits remains challenging



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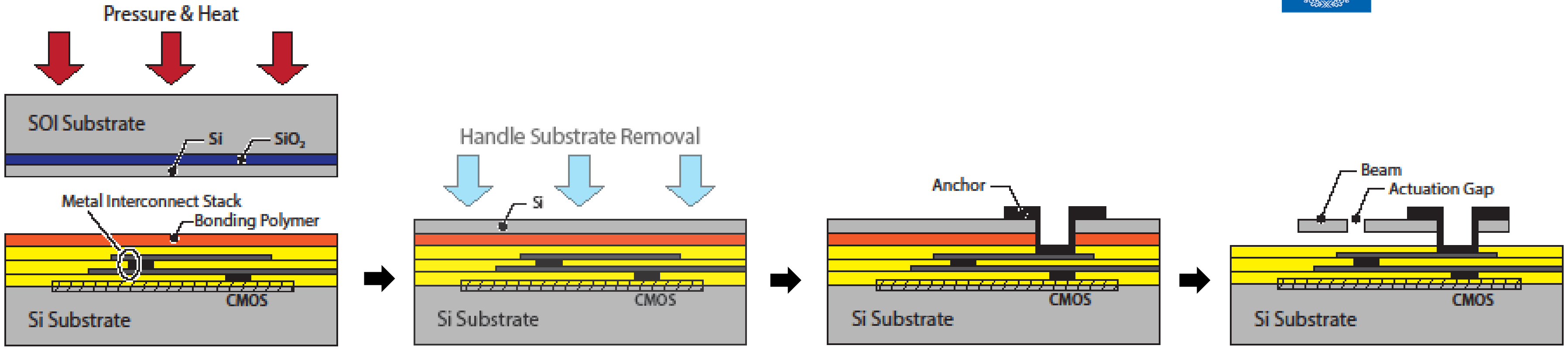
Where are we now…

- Process flow
  - Fabricate CMOS foundry wafer with interconnect stack
    - Commercially available foundry platform
  - Bond interconnect wafer to SOI / carrier wafer



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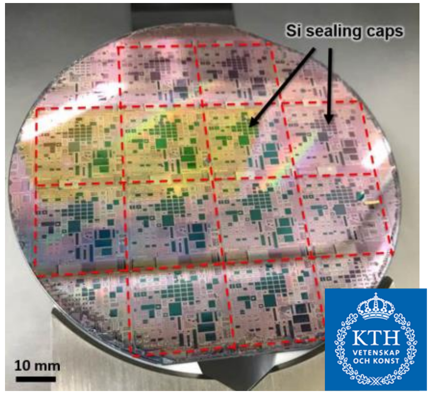
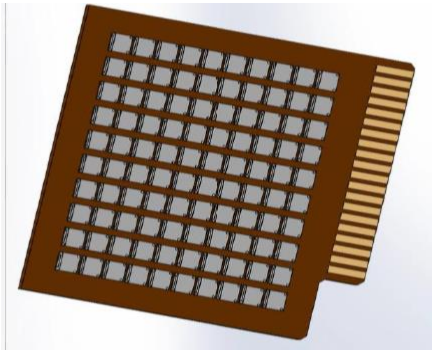
Where are we now…

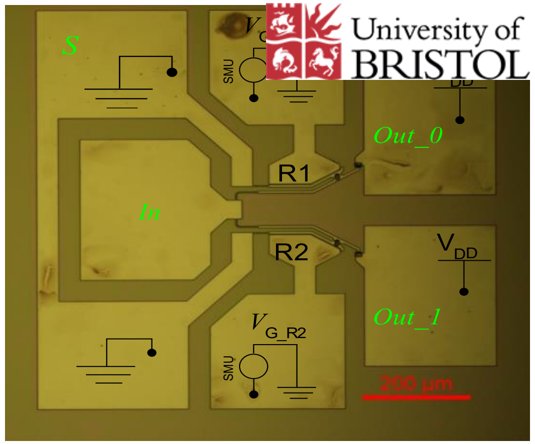
- Process flow (continued)
  - Structure NEM switches on SOI device layer
    - EBL or direct laser writing & reactive ion etching
  - Deposit contact layer and perform release etch
    - PECVD deposition of nanocrystalline graphite (NCG) & vapour phase HF etching
  - Characterisation/Failure mode and effect analysis (FMEA)
  - Packaging
  - Final characterization & FMEA

Where are we now…

- Demonstration of basic logic and memory functionality using our 3-T, 4-T and 7-T NEM relays
- Low to medium circuit complexity
- Development of temperature recording token
- Successful wafer level hermetic sealing of NEMS







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…and where do we want go to?

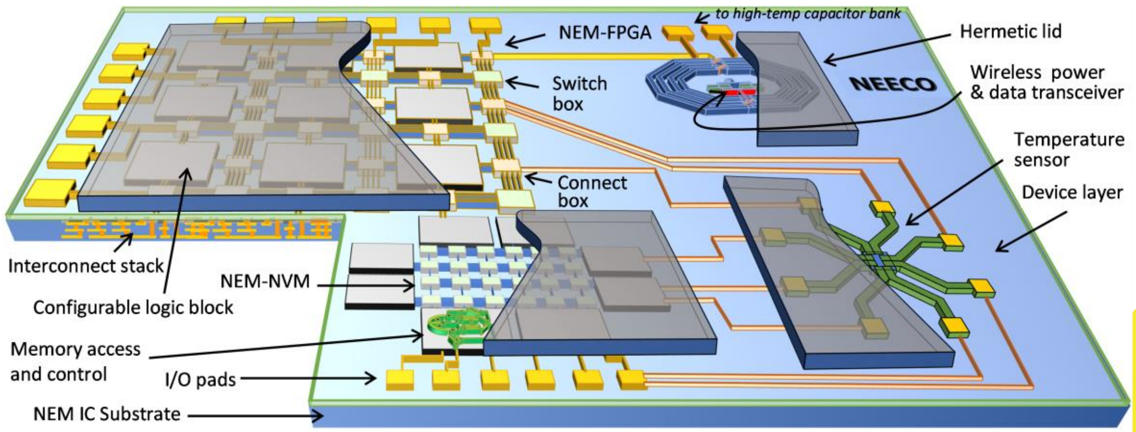
- End goal for the i-EDGE project, started Jan 1st 2023, the follow-up of ZeroAMP
  - Enable edge computing and sensing in harsh environements
  - Raise the technology readiness level (TRL) of our NEMS platform
  - Develop fabrication and integration approach to allow a step-by-step transfer to a foundry
    - Wafer scale processing
    - Replacing EBL & direct laser writing with high throughput optical lithography
    - Miniaturisation, reduction of critical dimensions (CD)
  - Increase integration density, improve yield
    - Hence, enable the fabrication of more complex NEMS circuits
    - These will include an FPGA, non-volatile memory blocks and logic
  - Full Systems-in-Package (SiP) and Systems-on-Chip (SoC) possible
  - Ultimately, commercialise the technology as a fabless start-up

Why a step-by-step transfer to a foundry?

- Some of the fabrication steps, e.g. the contact material deposition, are very specific to your technology platform
- Hence, these processes are currently not available as a commercial foundry service and may likely require substantial investments in tools
- Others, e.g. key lithography steps, can be transferred to a foundry as soon as designs for a certain CD node for our NEMS devices have been fully optimized and tested
- Each fabrication step which can be transferred to a commercial foundry not only helps to reduce costs, but will also increase the overall fabrication yield and reliability

How does this benefit sensor applications?

- Unique electronics for sensing in harsh environments not accessible for CMOS-based electronics
- PDK-based design toolkit available
- Complex circuits can be created using well-tested elements of a standard cell library
- Sensor integration either via a common interface or monolithically
- SiPs and SoCs with logic, memory, FPGA, wireless data and power transfer and sensor elements
- Hence, flexible platform for developing and testing novel sensors and sensing concepts in harsh environments



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